



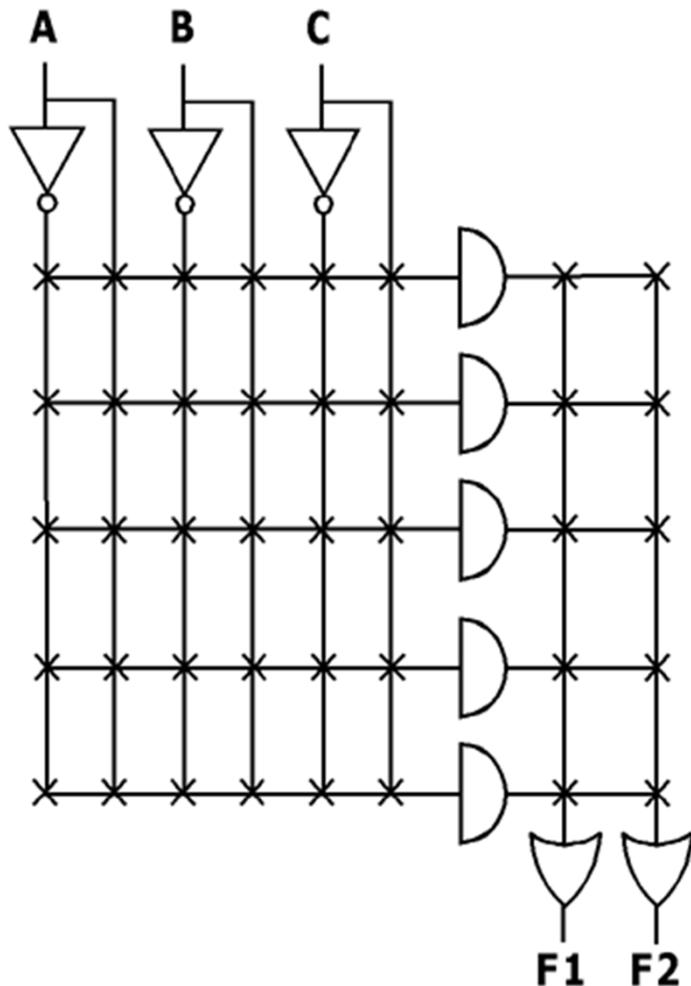
Digitalna tehnika

6. Vaja

Realizacija sinhronskih sekvenčnih vezij s
programirljivim vezjem FPGA



PLD – Programmable Logic Device

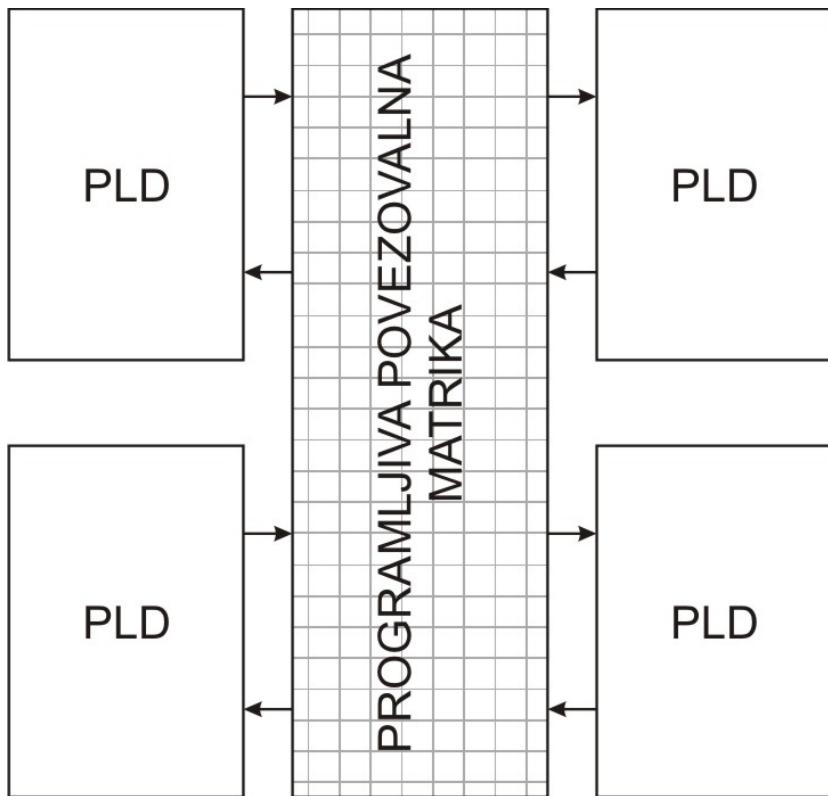


- PROM, EPROM, PLA, PAL, GAL
- Stiki povezav določajo končno funkcijo vezja
- Površina vezja se veča s kvadratom št. vhodov
- Nekaj 100 logičnih vrat

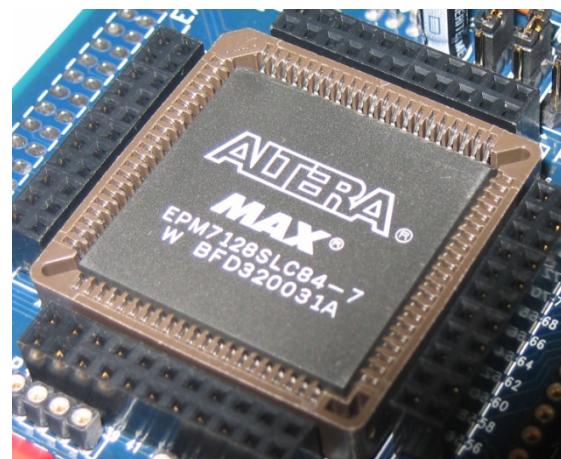




CPLD – Complex Programmable Logic Device

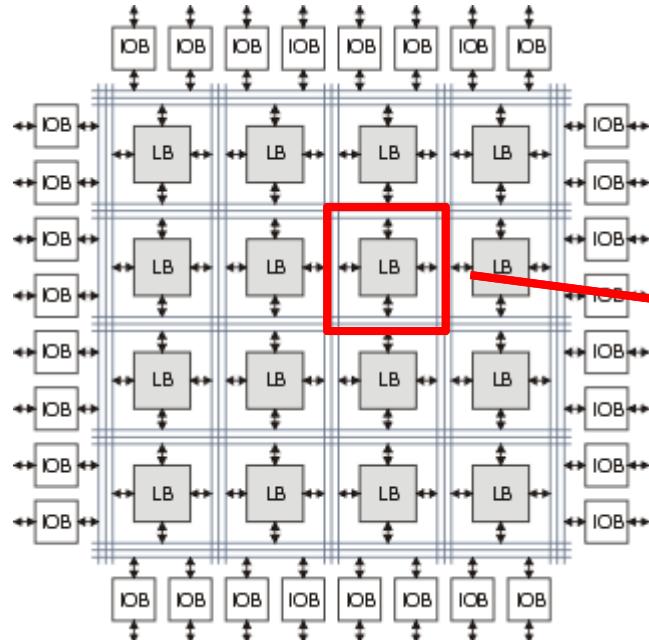


- Več blokov PLD povezanih s programljivo povezovalno matriko
- Izvedba kompleksnih logičnih funkcij
- Od 1000 do 100.000 logičnih vrat

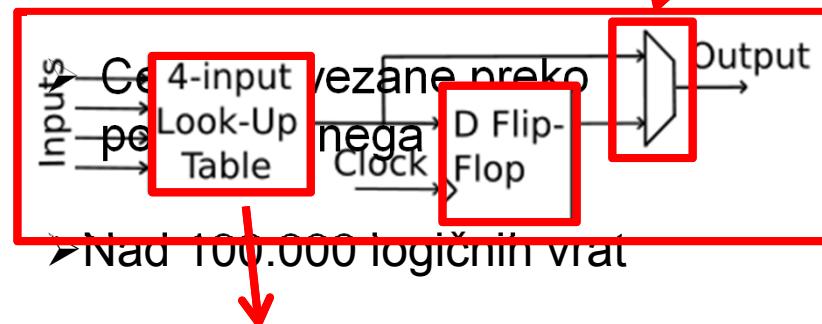




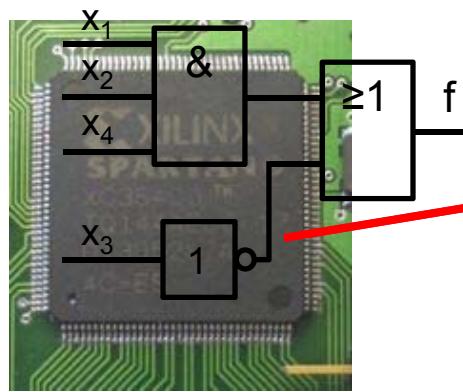
FPGA – Field Programmable Gate Array



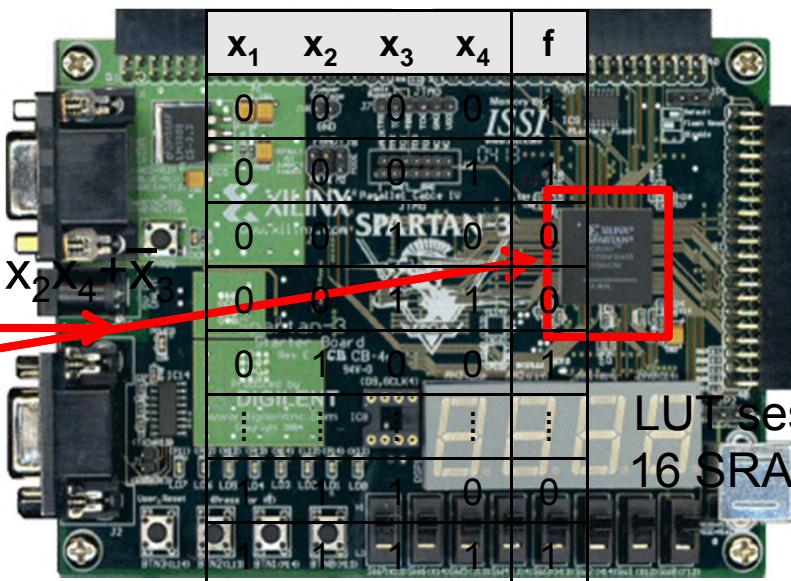
➤ Matrika logičnih celic (LB) obkroženih z vhodno/izhodnimi celicami



➤ Nad 100.000 logičnih vrat



$$f = x_1 x_2 x_4 + x_3$$



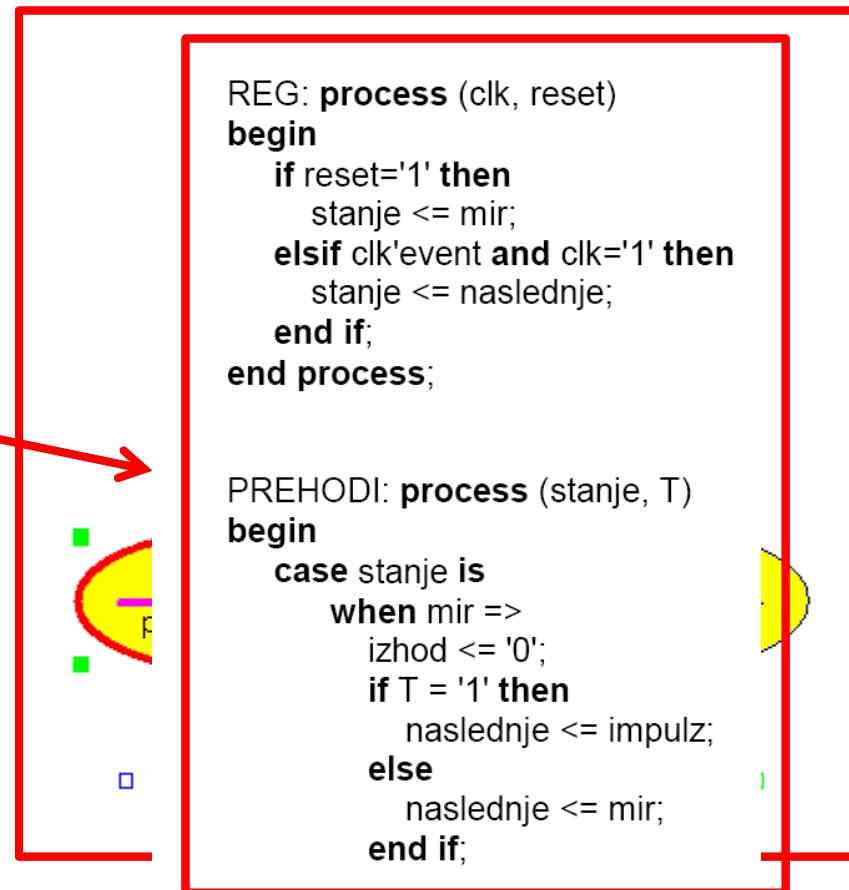
LUT sestavlja
16 SRAM celic



FPGA – Field Programmable Gate Array

NIVOJI MODELIRANJA

- Tranzistorji
- Logična vrata
- Nivo registrov
- Grafični modeli
- Obnašanje vezja
- Sistemski modeli



VHDL koda



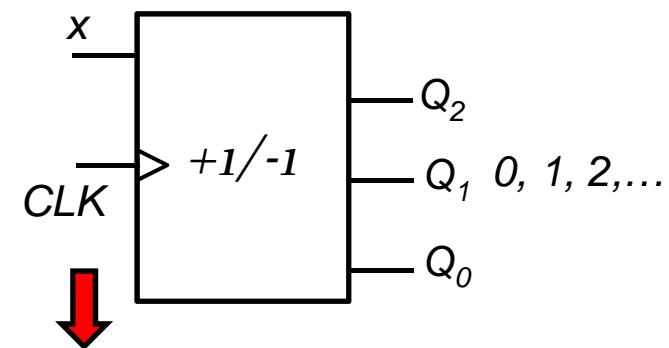
Naloge

6a: Z jezikom VHDL zapišite delovanje sinhronskega števca po modulu 5.

Uporabite stavka *process* in *if... then...else*

```
process (spremenljivke)
begin
:
sekvenčni stavki;
:
end process;
```

← { *if* izraz 1 *then*
stavki;
elsif izraz 2 *then*
stavki;
:
else izraz n;
end if;



Ukaz za proženje števca ob uri:

```
if (clk'event and clk='1') then
stavki;
end if;
```



Naloge

6b: Zapišite VHDL kodo za vezje, ki bo frekvenco CLK na plošči Xilinx zmanjšalo iz 50 MHz na 1 Hz.



6c: Zgradite sinhronsko sekvenčno vezje, ki bo vklapljalo smernike pri avtomobilu.



6d: Zgradite vezje, ki bo krmililo vrtenje koračnega motorčka..



VHDL
koda

Vaja6a

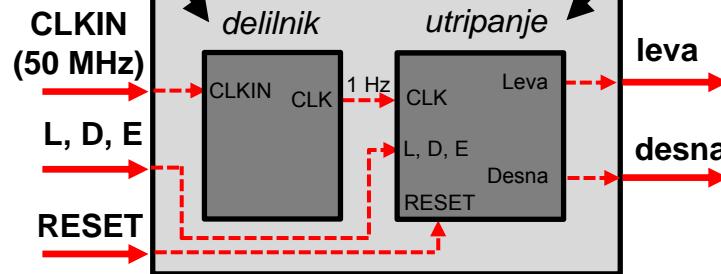
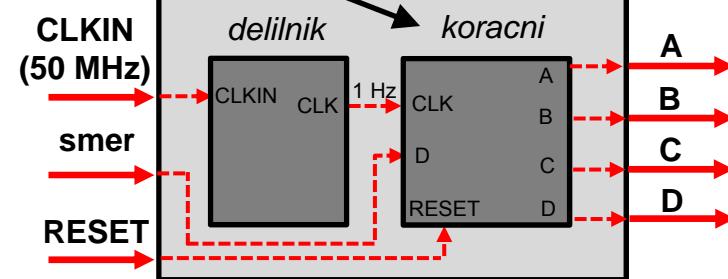


Diagram stanj
(StateCad)

Vaja6b

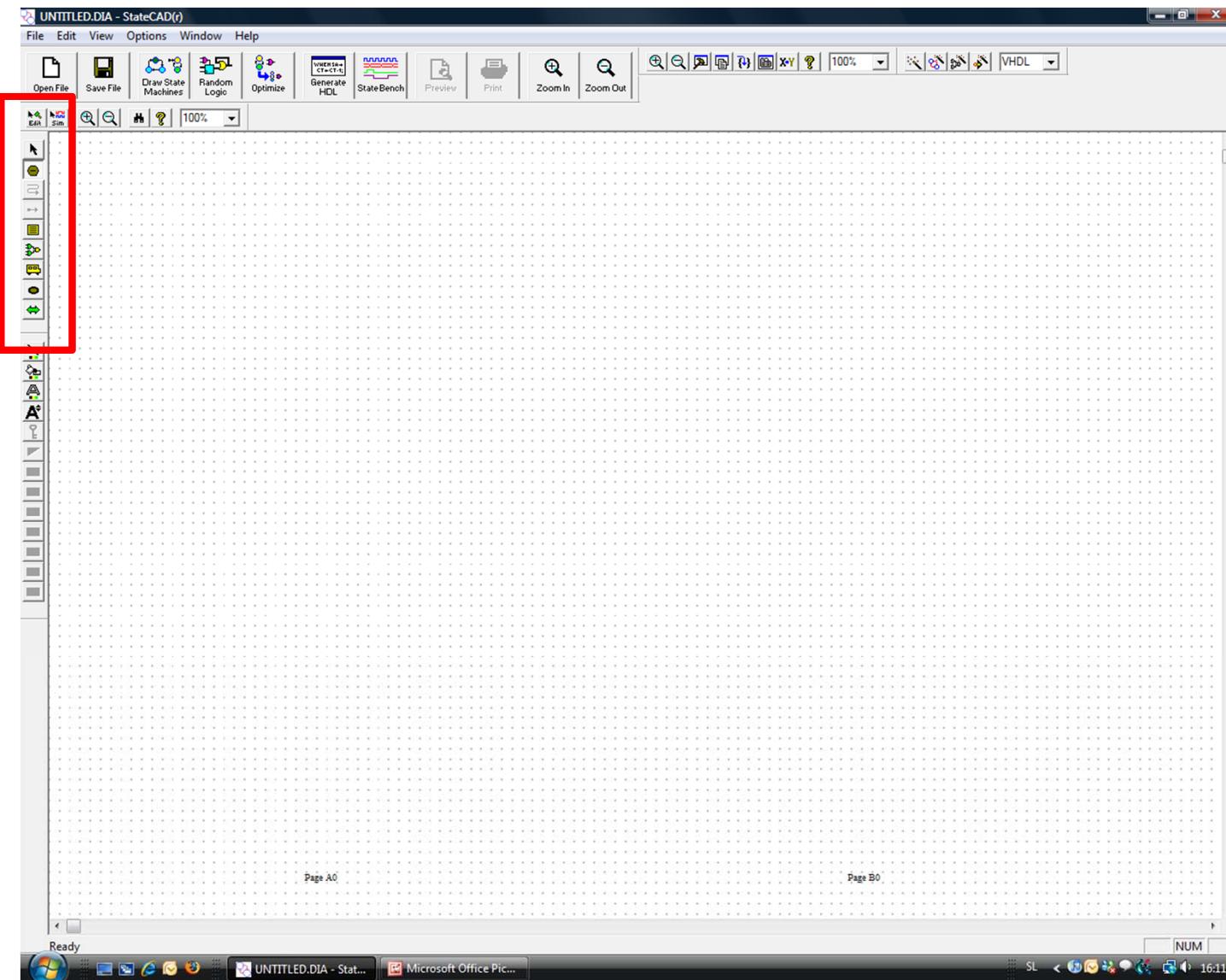


Vhodi: CLKIN, RESET, L, D, E
Izhodi: leva, desna

Vhodi: CLKIN, RESET, smer
Izhodi: A, B, C, D

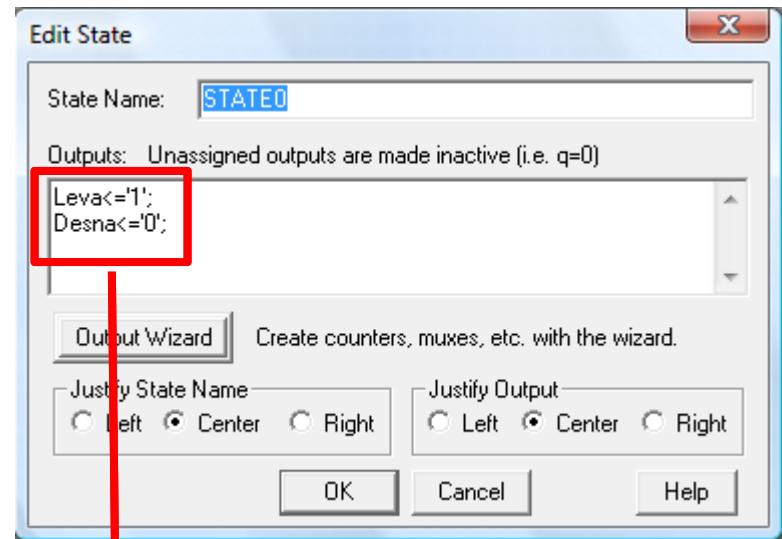
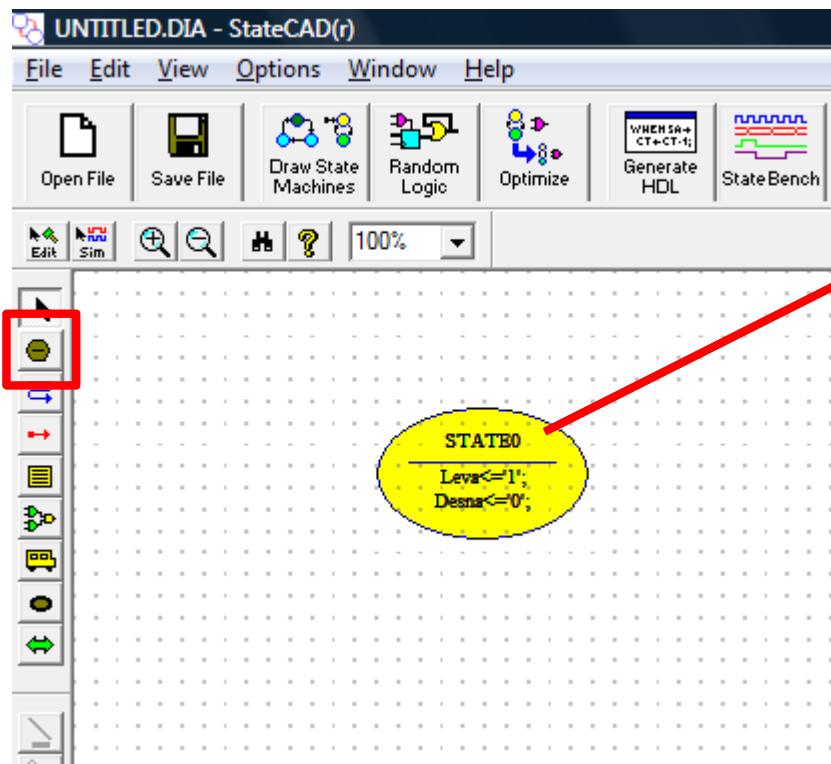


StateCAD





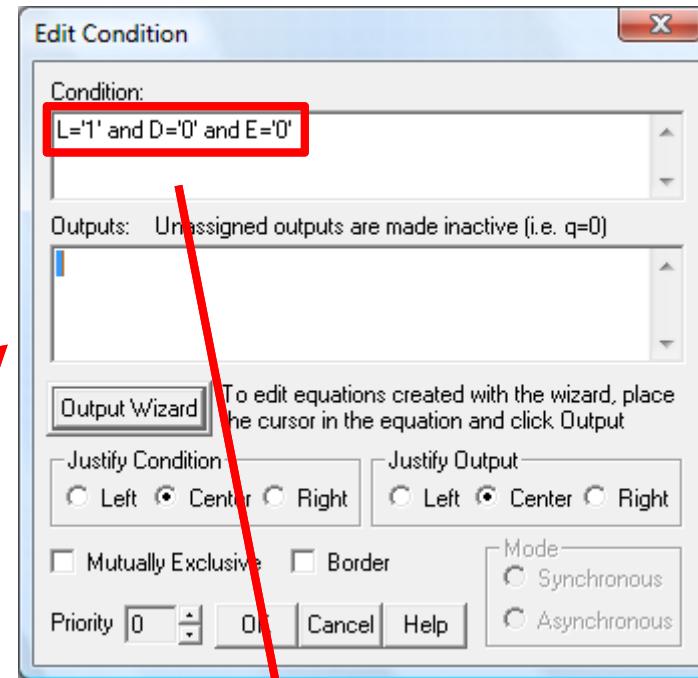
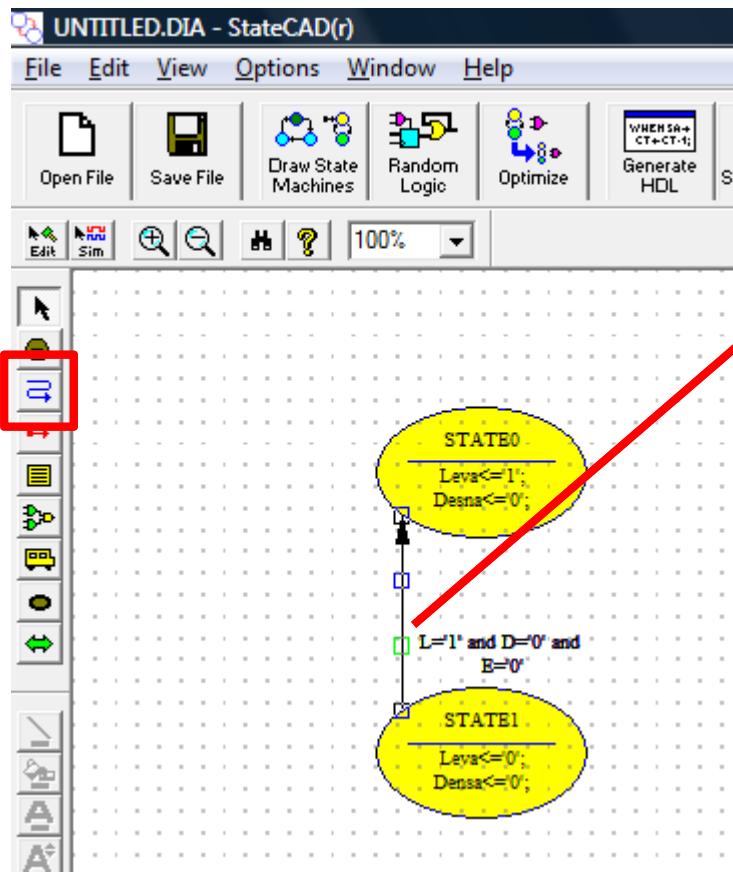
StateCAD – Definiranje stanj



Leva <= '1';
Desna <= '0';



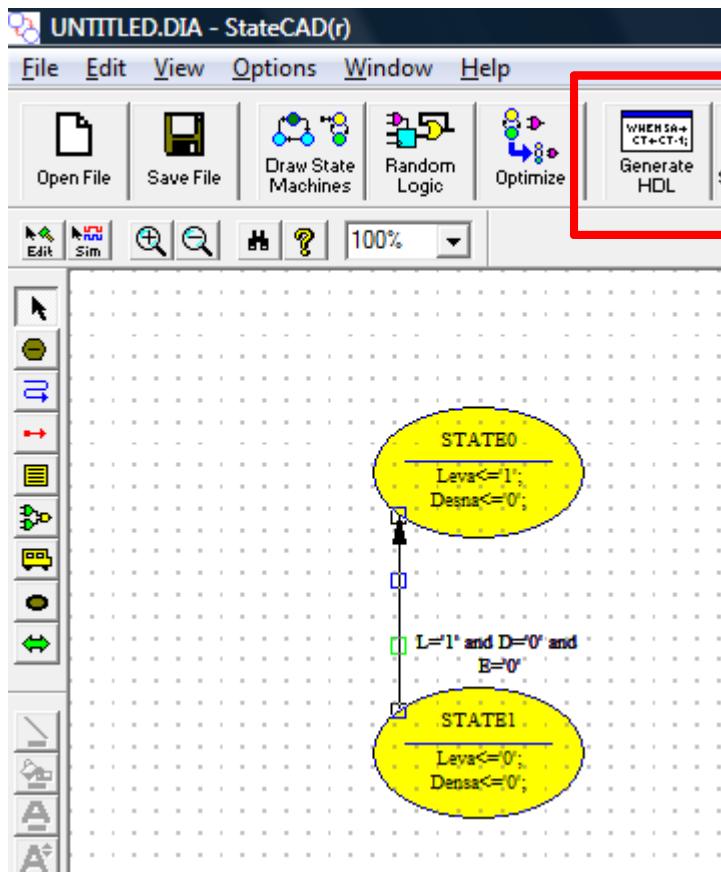
StateCAD – Definiranje prehodov



L='1' and D='0' and E='0'



StateCAD – Generiranje VHDL kode



Ko končamo z risanjem diagrama stanj, ga pretvorimo v VHDL kodo.



Xilinx ISE-predloga (Vaja7c in Vaja7d)

The screenshot shows the Xilinx ISE software interface with the following components:

- Sources Window:** Displays the project structure. The project is named "vaja7a" and contains a target device "xc3s200-4ft256". Inside the target device, there is a behavioral source file "vaja7a - Behavioral (vaja7a.vhd)" which includes two components: "component1 - delilnik" and "component2 - utripanje".
- Processes Window:** Shows available processes for the current design: Add Existing Source, Create New Source, View Design Summary, Design Utilities, User Constraints, Synthesize - XST, Implement Design, and Generate Programming File.
- VHDL Code Editor:** Displays the VHDL code for the "vaja7a" entity. The code defines the entity "vaja7a" with ports for clkin, reset, L, D, E (inputs) and leva, desna (outputs). It also defines an architecture "Behavioral" with a signal clk and two components: "component1: entity delilnik" and "component2: entity utripanje". The component2 port map includes connections for clk, reset, leva, desna, D, L, and E.

```
1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date: 12:06:44 01/07/2011
6  -- Design Name:
7  -- Module Name: vaja7a - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25 entity vaja7a is
26     Port (clkin, reset, L, D, E : in STD_LOGIC;
27             leva, desna : out STD_LOGIC);
28 end vaja7a;
29
30 architecture Behavioral of vaja7a is
31     signal clk:std_logic;
32
33 begin
34     component1: entity delilnik
35         port map(clkin=>clkin, clk=>clk);
36
37     component2: entity utripanje
38         port map(clk=>clk, reset=>reset, leva=>leva, desna=>desna, D=>D, L=>L, E=>E);
39
40 end Behavioral;
```



Xilinx ISE-predloga (Vaja7c in Vaja7d)

The screenshot shows the Xilinx ISE software interface with the following windows:

- Sources**: Shows the project structure under "Sources for: Synthesis/Implementation". It includes a folder "vaja7a" which contains an "xc3s200-4ft256" device and a "vaja7a - Behavioral (vaja7a.vhd)" source file. This file is expanded to show "component1 - delilnik - Behavioral (D:/svaru...)" and "component2 - UTRIPANJE - BEHAVIOR (D:/svaru...)".
- Processes**: Shows the available processes for the "vaja7a - Behavioral" source. The listed processes are: Add Existing Source, Create New Source, View Design Summary, Design Utilities, User Constraints, Synthesize - XST, Implement Design, and Generate Programming File.
- Code Editor**: Displays the VHDL code for the "vaja7a" entity. The code defines the entity "vaja7a" with ports for clkin, reset, L, D, E (inputs) and leva, desna (outputs). It also defines an architecture "Behavioral" with a begin block containing component instantiations for "delilnik" and "utripanje". A red bracket is drawn around the entire code area.

```
1  -----
2  --- Company:
3  --- Engineer:
4  ---
5  --- Create Date: 12:06:44 01/07/2011
6  --- Design Name:
7  --- Module Name: vaja7a - Behavioral
8  --- Project Name:
9  --- Target Devices:
10 --- Tool versions:
11 --- Description:
12 ---
13 --- Dependencies:
14 ---
15 --- Revision:
16 --- Revision 0.01 - File Created
17 --- Additional Comments:
18 ---
19 -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25 entity vaja7a is
26     Port (clkin, reset, L, D, E : in STD_LOGIC;
27             leva, desna : out STD_LOGIC);
28 end vaja7a;
29
30 architecture Behavioral of vaja7a is
31 signal clk:std_logic;
32
33 begin
34 component1: entity delilnik
35 port map(clkin=>clkin, clk=>clk);
36
37 component2: entity utripanje
38 port map(clk=>clk, reset=>reset, leva=>leva, desna=>desna, D=>D,L=>L,E=>E);
39
40 end Behavioral;
```



LABORATORIJ ZA BIOKIBERNETIKO

FAKULTETA ZA ELEKTROTEHNIKO UNIVERZA V LJUBLJANI

Za to vajo ni potrebno izdelati poročila.