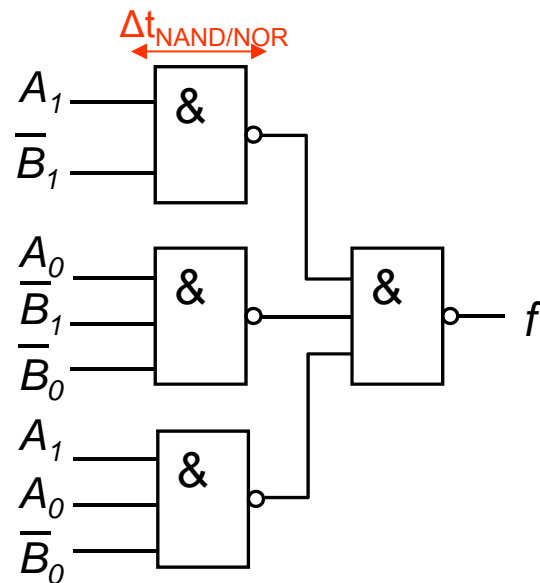


Digitalne strukture

3. Vaja

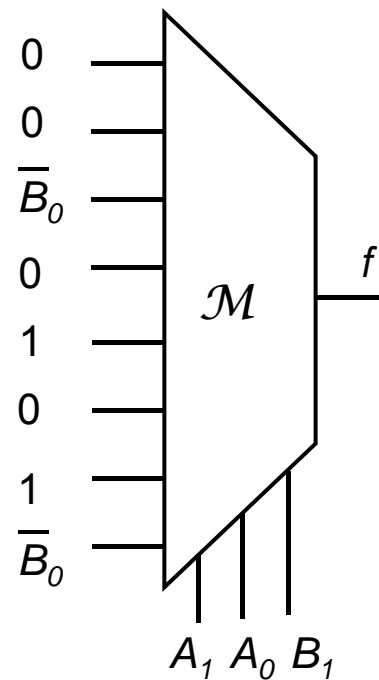
Simulacija delovanja kombinacijskih vezij (P-SPICE)

Naloga 3a: Simulacija dvobitnega primerjalnika z NAND/NOR:



Naloga 3b: Zakasnitev ("propagation delay") vrat NAND/NOR - $\Delta t_{\text{NAND/NOR}}$

Naloga 3c: Simulacija dvobitnega primerjalnika z multipleksorjem 74HC151:



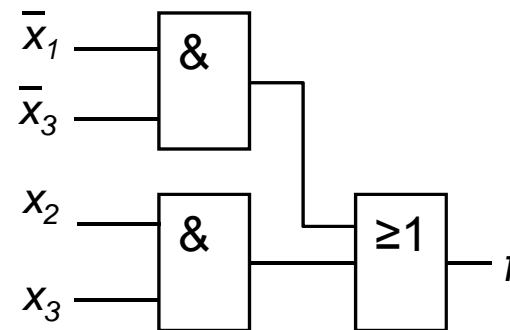
Naloga 3d: Statični hazard v vezjih AND-OR oz. OR-AND:

$$f(x_1, x_2, x_3) = \sum 0, 2, 3, 7$$

Naloga 3d: Statični hazard v vezjih AND-OR oz. OR-AND:

$$f(x_1, x_2, x_3) = \sum 0, 2, 3, 7$$

| | | $x_1 x_2$ | | | |
|-------|---|-----------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| x_3 | 0 | 1 | 1 | | |
| | 1 | | 1 | 1 | |

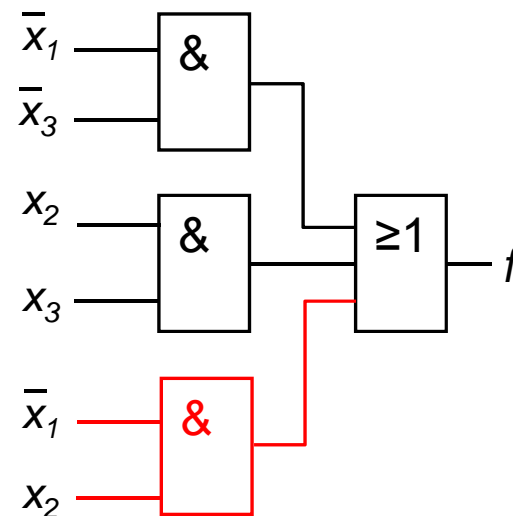


Časovni diagram: pri kateri spremembi vhodov se pojavi hazard?

Naloga 3d: Statični hazard v vezjih AND-OR oz. OR-AND:

$$f(x_1, x_2, x_3) = \sum 0, 2, 3, 7$$

| | | $x_1 x_2$ | | | |
|-------|---|-----------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| x_3 | 0 | 1 | 1 | | |
| | 1 | | 1 | 1 | |



Naloga 3e: Odprava hazarda:

| | | $x_1 x_2$ | | | |
|-------|---|-----------|----|----|----|
| | | 00 | 01 | 11 | 10 |
| x_3 | 0 | 1 | 1 | | |
| | 1 | | 1 | 1 | |

OrCAD (PSpice)

The screenshot displays the OrCAD Capture software interface. The main workspace is a grid with a toolbar on the left containing various symbols and tools. Three arrows point to specific tools in the toolbar with the following labels:

- povezave (connections)
- imena povezav (connection names)
- stičišče (junction)

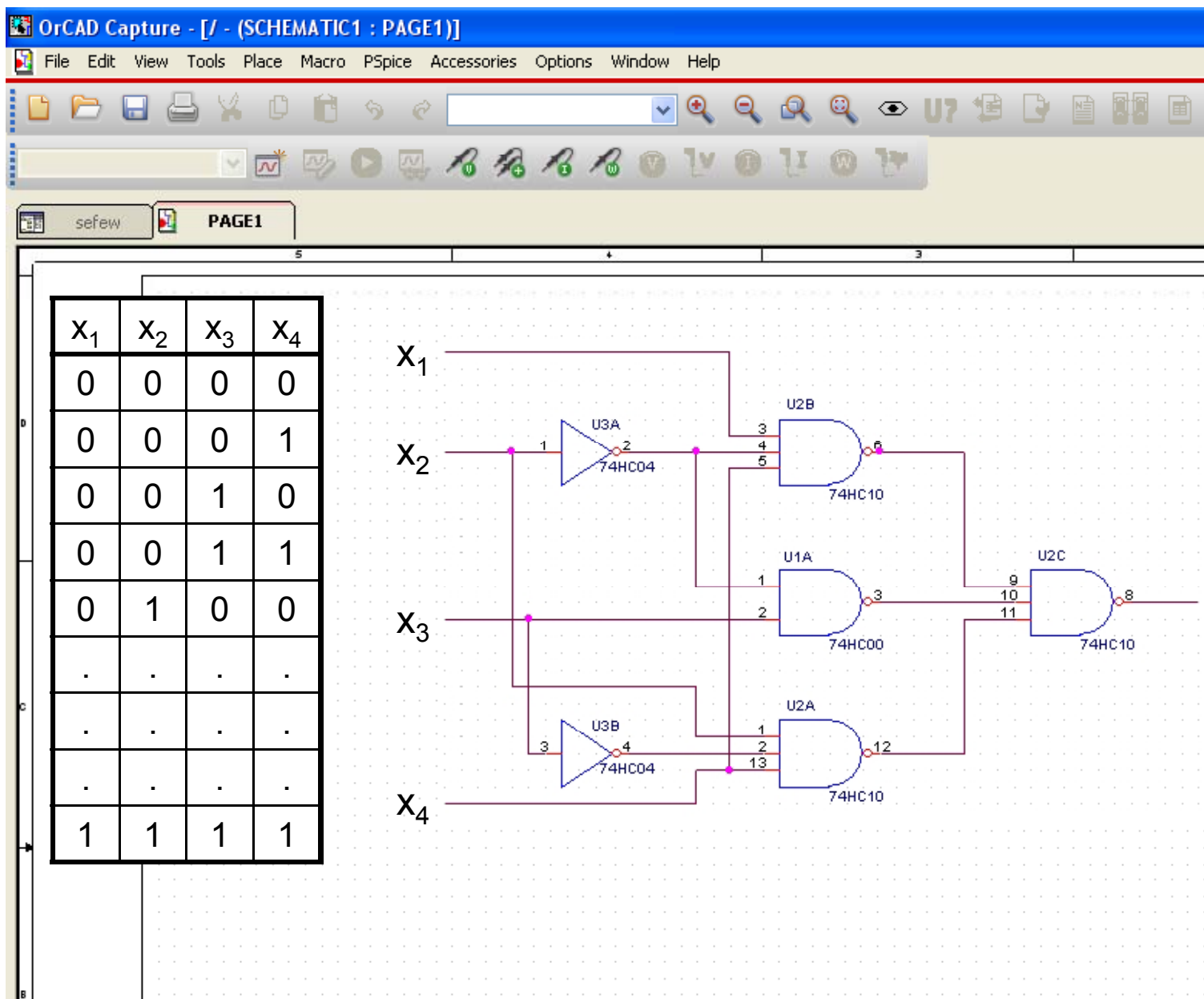
The 'Place Part' dialog box is open on the right, showing the following details:

- Part: 74HC00
- Part List: 74HC00, 74HC01, 74HC02, 74HC03, 74HC04, 74HC05, 74HC08, 74HC09
- Libraries: 74HC, Design Cache, SOURCE
- Packaging: Parts per Pkg: 4, Part: A, Type: Homogeneous
- Normal (selected) / Convert
- Search for Part

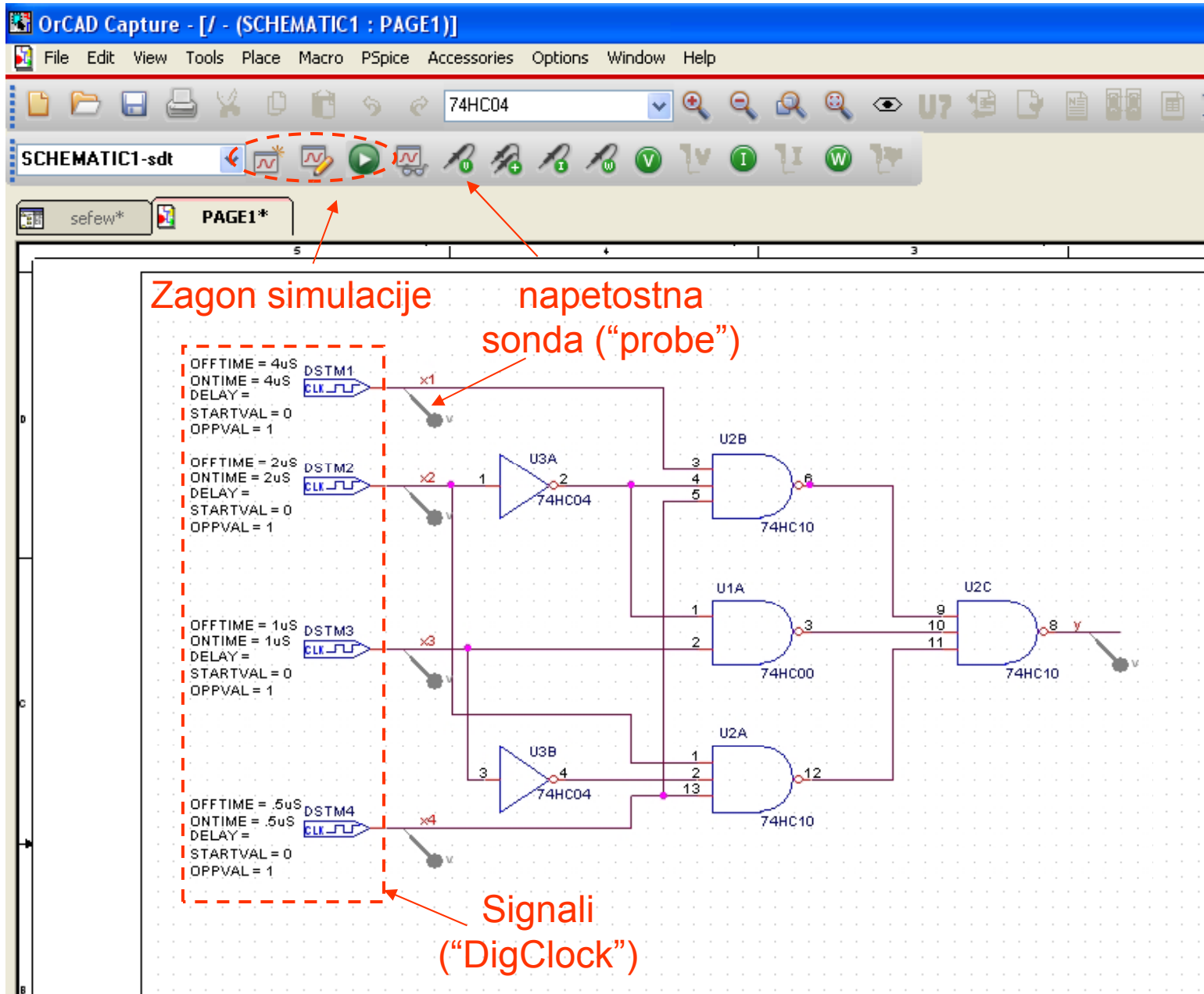
A schematic symbol for a NAND gate is shown in the dialog, labeled 'U?A' and '74HC00'. The status bar at the bottom indicates '0 items selected' and 'Scale=106% X=3.50 Y=3.00'.

| | | |
|-------|--------------------------|----------------|
| Title | <Title> | |
| Size | Document Number | Rev <Rev Code> |
| A | <Doc> | |
| Date: | Sunday, October 17, 2010 | Sheet 1 of 1 |

Vezje

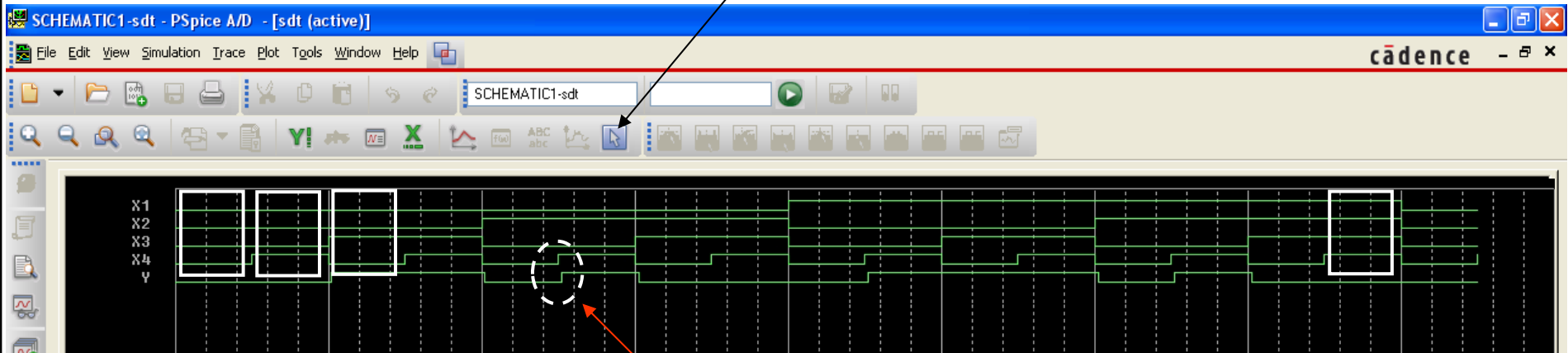


Vhodni
signali
in sonde



Rezultati simulacije (časovni diagram)

kurzorji



zakasnitev

| X ₁ | X ₂ | X ₃ | X ₄ | y |
|----------------|----------------|----------------|----------------|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| . | . | . | . | |
| . | . | . | . | |
| . | . | . | . | |
| 1 | 1 | 1 | 1 | 0 |

Poročilo

- ❑ Besedilo vaje
- ❑ Časovni diagram vhodnih in izhodne spremenljivke (*primerjalnik*)
- ❑ Zakasnitev na vratih NAND/NOR
- ❑ Časovni diagram izhodne funkcije vezja s hazardom